This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Please cancel claims 1-28 without prejudice or disclaimer.

Claims 1-28 (Cancelled)

29. (Original) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type, having a main surface and a back surface;

a power MOSFET formed in the semiconductor substrate; and

a peripheral device formed in the semiconductor substrate,

wherein the power MOSFET comprises:

a drift region of the first conductivity type extending in the semiconductor substrate from the main surface in a perpendicular direction with respect to the main surface;

a base region of a second conductivity type extending in the drift region from the main surface in the perpendicular direction;

a source region of the first conductivity type extending in the base region from the main surface in the perpendicular direction;

a trench extending from the main surface in the perpendicular direction, and penetrating the base region from the source region to the drift region;

a gate insulating film provided on an inner wall of the trench; and

a gate electrode provided on a surface of the gate insulating film and filling an inside of the trench, and

wherein the peripheral device is a first conductivity type channel MOSFET, and comprises:

a well layer of the first conductivity type extending in the semiconductor substrate from the main surface in the perpendicular direction;

a base region of the second conductivity type extending in the well layer from the main surface in the perpendicular direction;

a semiconductor region of the first conductivity type extending in the base region from the main surface in the perpendicular direction;

a trench extending from the main surface in the perpendicular direction and dividing the semiconductor region into a source region and a drain region;

a gate insulating film provided on an inner wall of the trench; and

a gate electrode provided on a surface of the gate insulating film and filling an inside of the trench.

30. (Original) The semiconductor device according to claim 29, wherein the semiconductor device is manufactured by:

forming the drift region of the power MOSFET and the well layer of the peripheral device simultaneously;

forming the base region of the power MOSFET and the base region of the peripheral device simultaneously;

forming the source region of the power MOSFET and the semiconductor region of the peripheral device simultaneously;

forming the trench of the power MOSFET and the trench of the peripheral device simultaneously;

forming the gate insulating film of the power MOSFET and the gate insulating film of the peripheral device simultaneously; and

forming the gate electrode of the power MOSFET and the gate electrode of the peripheral device simultaneously.

31. (Original) The semiconductor device according to claim 29, further comprising first and second peripheral devices each of which is the first conductivity type channel MOSFET comprising the well layer, the base region, the semiconductor region divided into the source region and the drain region by the trench, the gate insulating film and the gate electrode, wherein:

the base region of the first peripheral device and the base region of the second peripheral device are electrically separated from each other by an isolation trench extending from the main surface in the perpendicular direction, an insulating film provided on an inner wall of the isolation trench, and a poly silicon layer provided on a surface of the isolation insulating film and filling the isolation trench.

32. (Original) The semiconductor device according to claim 31, wherein the semiconductor device is manufactured by;

forming the trench of each of the first and second peripheral devices and the isolation trench simultaneously;

forming the gate insulating film of each of the first and second peripheral devices and the isolation insulating film simultaneously; and

forming the gate electrode of each of the first and second peripheral devices and the poly silicon layer simultaneously.

33. (Original) The semiconductor device according to claim 29, wherein the peripheral device further includes a second conductivity type channel MOSFET comprising:

a trench extending in the well layer from the main surface in the perpendicular direction;

a gate insulating film provided on an inner wall of the trench;

a gate electrode provided on a surface of the gate insulating film and filling the trench;

a source region of the second conductivity type extending in the well layer from the main surface in contact with the gate insulating film at a side of the trench; and

a drain region of the second conductivity type extending in the well layer from the main surface in contact with the gate insulating film at the side of the trench, the drain being separated from the source region.

34. (Original) The semiconductor device according to claim 33, wherein the source region and the drain region of the second conductivity type channel MOSFET are provided at both sides of the trench thereof.

35. (Original) The semiconductor device according to claim 33, wherein, in the second conductivity type channel MOSFET, the source region surrounds a first end portion of the trench, and the drain region surrounds a second end portion of the trench opposite to the first end portion in a direction parallel to the main surface of the semiconductor substrate.

36. (Original) The semiconductor device according to claim 29, the power MOSFET further includes a high-concentration contact region of the second conductivity type extending in the base region from the main surface in the perpendicular direction and having an impurity concentration higher than that of the base region.

37. (Original) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type, having a main surface and a back surface;

a power MOSFET formed in the semiconductor substrate; and

a peripheral device formed in the semiconductor substrate,

wherein the power MOSFET comprises:

a drift region of the first conductivity type extending in the semiconductor substrate from the main surface in a perpendicular direction with respect to the main surface;

a base region of a second conductivity type extending in the drift region from the main surface in the perpendicular direction;

a source region of the first conductivity type extending in the base region from the main surface in the perpendicular direction;

a trench extending from the main surface in the perpendicular direction, and penetrating the base region from the source region to the drift region;

a gate insulating film provided on an inner wall of the trench; and

a gate electrode provided on a surface of the gate insulating film and filling an inside of the trench, and

wherein the peripheral device is a second conductivity type channel MOSFET, and comprises:

a well layer of the first conductivity type extending in the semiconductor substrate from the main surface in the perpendicular direction, and having an impurity concentration lower than that of the semiconductor substrate;

a trench extending in the well layer from the main surface in the perpendicular direction;

a gate insulating film provided on an inner wall of the trench;

a gate electrode provided on a surface of the gate insulating film and filling the trench;

a source region of the second conductivity type extending in the well layer from the main surface in contact with the gate insulating film at a side of the trench; and

a drain region of the second conductivity type extending in the well layer from the main surface in contact with the gate insulating film at the side of the trench, the drain region being separated from the source region.

38. (Original) The semiconductor device according to claim 37, wherein the power MOSFET further comprises a high-concentration contact region of the second conductivity type extending in the base region from the main surface in the perpendicular direction and having an impurity concentration higher than that of the base region.

39. (Original) The semiconductor device according to claim 38, manufactured by:

forming the drift region of the power MOSFET and the well layer of the peripheral device simultaneously;

forming the high-concentration contact region of the power MOSFET and the source region and the drain region of the peripheral device simultaneously;

forming the trench of the power MOSFET and the trench of the peripheral device simultaneously;

forming the gate insulating film of the power MOSFET and the gate insulating film of the peripheral device simultaneously; and

forming the gate electrode of the power MOSFET and the gate electrode of the peripheral device simultaneously.

40. (Original) The semiconductor device according to claim 37, wherein the source region and the drain region of the second conductivity type channel MOSFET are provided at both sides of the trench thereof.

41. (Original) The semiconductor device according to claim 37, wherein, in the second conductivity type channel MOSFET, the source region surrounds a first end portion of the trench, and the drain region surrounds a second end portion of the trench opposite to the first end portion in a direction parallel to the main surface of the semiconductor substrate.

42. (Original) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type and having a main surface with a first area where a power MOSFET is provided and a second area where a peripheral device is provided;

first and second semiconductor regions of the first conductivity type, respectively provided in the semiconductor substrate at the first area and the second area and having impurity concentrations approximately equal to each other and lower than that of the semiconductor substrate;

first and second trenches respectively extending in the first and second semiconductor regions and having depths approximately equal to each other;

first and second insulating films respectively provided on inner walls of the first and second trenches; and

first and second conductive members respectively filling the first and second trenches with the first and second insulating films interposed therebetween, wherein:

the power MOSFET is composed of the first semiconductor region as a drift region, a base region of a second conductivity type extending in the drift region, a source region of the first conductivity type extending in the base region, the first insulating film as a gate insulating film, and the first conductive member as a gate electrode that extends to face the drift region, the base region, and the source region via the gate insulating layer; and

the peripheral device is a MOSFET composed of the second semiconductor region as a well layer, the second insulating film as a gate insulating film, the second conductive member as a gate electrode, source and drain regions provided in the well layer separately from each other, the source and drain regions facing the gate electrode with the gate electrode interposed therebetween.

43. (Original) The semiconductor device according to claim 42, wherein:

the peripheral device is a first conductivity type channel MOSFET, and further includes a base region of the second conductivity type having a depth approximately equal to that of the base region of the power MOSFET; and

the source and drain regions of the peripheral device are of the first conductivity type and have a depth approximately equal to that of the source region of the power MOSFET.

~~43.~~44. (Currently amended) The semiconductor device according to claim 42, wherein:

the peripheral device is a second conductivity type channel MOSFET; and

the source and drain regions of the peripheral device are of the second conductivity type.